

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

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Serial No.

Filed: September 4, 2001

For: SEMICONDUCTOR DEVICE

1-13-02

PRELIMINARY AMENDMENTCommissioner for Patents
Washington, D.C. 20231

Sir:

Prior to examination, please amend the above-identified application as follows.

IN THE CLAIMS

Rewrite claim 10 as follows:

10. (Amended) A semiconductor memory cell in a memory cell array, comprising:

the semiconductor memory cells as defined in claim 5, being aligned in plural numbers thereof, wherein they are driven by a data line and word line, wherein:

drain regions of plural numbers of semiconductor memory cells are connected to a same data line;

second gates of said plural numbers of said semiconductor memory cells, which are connected to the same data line at said drain regions thereof, are connected with each other; and